AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 7, line 6, with the following amended paragraph:

If any instruction generates a recoverable error, the processor 100 provides precise trap handling by returning to its machine state at the time the exception occurred, and resuming operation. When a precise trap occurs, the processor 100 ensures a precise state by completing execution of all instruction packets issued before the one that induced the trap. In addition, the processor 100 prevents all instruction packets that issued after [[that]] the one that induced the trap from completing execution, even if they finished out of order before the trap-inducing instruction. The processor 100, therefore, restores itself to its state at the time of the exception. After such restoration, execution may be resumed. Operation may either be resumed from the trapping instruction or from the instruction following the trapping instruction. In this manner the processor 100 provides that instructions that finish out of order with respect to other packet instructions, or other packets, and then generate an exception, will nonetheless allow the processor 100 to resume operation at a precise state, as long as the error is a recoverable error (i.e., the error does not prevent restoration of the exception-time machine state).

Please replace the paragraph beginning on page 8, line 24, with the following amended paragraph:

If a match is not found, then the new instruction [[is]] enters the scoreboard 600 at the first invalid scoreboard entry corresponding to load instructions. The number of entries in the scoreboard allocated for unfinished loads is equal to the number of entries in the load buffer 400 (FIGURE 4) of the LSU 218, described below.